CLAIMS

What is claimed is:

1. A charge trapping dielectric memory device, comprising:

a substrate having a first conductive region and a second conductive region formed therein and a channel region interposed between the first and the second conductive regions;

a first dielectric layer disposed over the substrate;

a dielectric charge trapping layer disposed over the first dielectric layer;

a second dielectric layer disposed over the charge trapping layer; and

a gate electrode disposed over the second dielectric layer, wherein the gate electrode has a work function of about 4.6 eV to about 5.2 eV.

2. The memory device according to claim 1, wherein the gate electrode has a work function of about 4.6 eV to about 4.9 eV.

3. The memory device according to claim 1, wherein the gate electrode is implemented as a word line.

4. The memory device according to claim 1, wherein the first and second conductive regions are implemented as buried bit lines.

5. The memory device according to claim 1, wherein the gate electrode is made from nickel silicide (NiSi).

6. The memory device according to claim 1, wherein the gate electrode is made from tungsten (W).

7. The memory device according to claim 1, wherein the gate electrode is made from cobalt silicide (CoSi).

8. The memory device according to claim 1, wherein the gate electrode is made from P+ silicon carbide (SiC).

9. The memory device according to claim 1, wherein the thickness of the first dielectric layer is less than the thickness of the second dielectric layer.

10. The memory device according to claim 9, wherein the first dielectric layer has a thickness of about 40Å to about 60Å.

11. The memory device according to claim 10, wherein the second dielectric layer has a thickness of about 100Å to about 120Å.

12. The memory device according to claim 9, wherein the first dielectric layer is effective to (i) increase the probability that, during an erase operation, electrons within the charge trapping layer will overcome a potential barrier of the first dielectric layer to exit the charge trapping layer into the substrate, and (ii) decrease the probability that, during operations other than an erase operation, electrons will overcome a potential barrier of the first dielectric layer and escape from the charge trapping layer.

13. The memory device according to claim 9, wherein the work function of the gate electrode and the first dielectric layer are effective to increase the probability that electrons will be removed from the charge trapping layer via a channel erase operation.

14. The memory device according to claim 1, wherein the work function of the gate electrode is effective to decrease the probability that, during an erase operation, electrons within the gate electrode will overcome a potential barrier of the second dielectric layer and enter the charge trapping layer.

15. The memory device according to claim 1, wherein the charge trapping layer is effective to store distinct charge amounts in each of a first and a second

charge trapping region, the each distinct charge amount selected from a plurality of charge levels.

16. A method of performing an erase operation on a non-volatile, charge trapping dielectric memory device having a source and a drain within a substrate, a first dielectric layer disposed over the substrate, a dielectric charge trapping layer disposed over the first dielectric layer, a second dielectric layer disposed over the charge trapping layer, and a gate electrode disposed over the second dielectric layer to define a channel between the source and the drain, the memory device having been programmed by trapping charge in at least one charge trapping region of the dielectric charge trapping layer, the method comprising the simultaneous steps of:

applying a negative erase voltage to a gate electrode, the gate electrode having a work function of about 4.6 eV to about 5.2 eV;

one of (i) connecting the drain to a zero potential, and (ii) floating the drain;

one of (i) connecting the source to a zero potential and (ii) floating the source; and

connecting the substrate to a zero potential.

17. The method according to claim 16, wherein the erase voltage applied to the gate is in a range of about -10 volts to about -20 volts.

18. The method according to claim 16, wherein the charge trapping layer includes two charge trapping regions and both bits are erased simultaneously.

19. The method according to claim 16, wherein the gate electrode has a work function of about 4.6 eV to about 4.9 eV.

20. The method according to claim 16, wherein the stored charge is selected from one of a plurality of charge levels.